REMARKS

Claims 1-12, 56-59 and 77-84 remain rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (5,939,871). Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Shinada (5,708,571). The rejections are respectfully traversed and reconsideration is requested.

Please refer to the discussion of this rejection presented in the last response. Note however, that at page 3, second paragraph, the undersigned misspoke. With the diode D of Tanaka, the load current, on average, would not go below zero as suggested by that discussion.

In response to the arguments of the last response, the Examiner stated:

> The crux of applicant's argument is that the diode of the cited prior art Tanaka is being used to control the minimum current. This is an incorrect reading of the circuit. First the diode is a passive element. The diode cannot function to control anything because it cannot turn on or off nor can it sense any current. The cited comparators 3 and 4 served to sense the output current by sending this sensed value to the control circuit and thereby effectively control the minimum current limit at the output.

Although it is agreed that the passive diode cannot be termed an override control responsive to a condition of the power converter to effect a minimum current limit, the diode can limit current in a passive manner. The following discussion should clarify Applicant's position.

Please refer to Figs. 3 and 5A of Tanaka. Transistor 1 is turned on by the control circuit 7 at time T_1 and conducts until peak current I_{Lr} is sensed by comparator 3 at T_2. Between T_1 and T_2, current flows through the inductor L. Diode D is reverse biased and thus does not conduct. Between times T_2 and T_3, the inductor L continues to drive current to a capacitor C, the current being drawn from ground through diode D. The current ramps down until time T_3 at zero amps. Current would continue negative except that the diode D does not conduct in the reverse direction. In this example, zero current is also sensed at T_3 by comparator 4, but as previously explained, the

only response of the control circuit 7 is to begin monitoring the output voltage. The next control point is at T_4 when the output voltage crosses the set output voltage level.

As discussed above, it is the diode D that prevents negative current flow through the inductor I. It happens in the example presented at column 4, lines 16 and 17, that the sensed current I_{LB} is set to zero, which matches the current limit determined by the diode D. However, the control circuit 7 does not effect a minimum current limit as can be seen by the cases where I_{LB} does not equal to zero presented in the attached sketches. (The voltage waveforms represented in the sketches would not actually follow straight lines as illustrated but have been presented as such in keeping with Fig. 5 of Tanaka.)

In Sketch 1, the minimum current is set at a level greater than zero. At time T_3, the level I_{LB} is sensed and the control circuit is caused to monitor the voltage as before. However, because the current has not yet reached zero, the limit set by the diode D, the current continues to fall. The current does not reverse until time T_4 when the voltage is sensed to cross the set output voltage. In this case, there is no limit to current.

In Sketch 2, the current level I_{LB} is again set greater than zero. In this case, however, the current does reach zero before time T_4. Accordingly, the diode does limit current to zero volts well below the sensed current I_{LB}.

In Sketch 3, I_{LB} is set less than zero. This example would be non-operational using the diode D, because the current would be limited by diode D at zero before it ever drops to the negative level I_{LB}. However, if the diode were replaced by a synchronous rectifier as suggested at the top of column 13, negative current would be allowed. In that case, the negative current limit would be sensed at T_3, but the current would continue to become more negative until the voltage crossed the set output voltage at time T_4. Accordingly, the current would not be limited to I_{LB}.

From the above examples, it should be recognized that it is the passive diode D that limits current in Tanaka and not the control circuit 7. Accordingly, there is no "override control to the control circuit, responsive to a condition of the power converter or connected circuitry, that

increases the output voltage to effect a minimum current limit of the output current at the output terminals" as required, for example, by claim 1.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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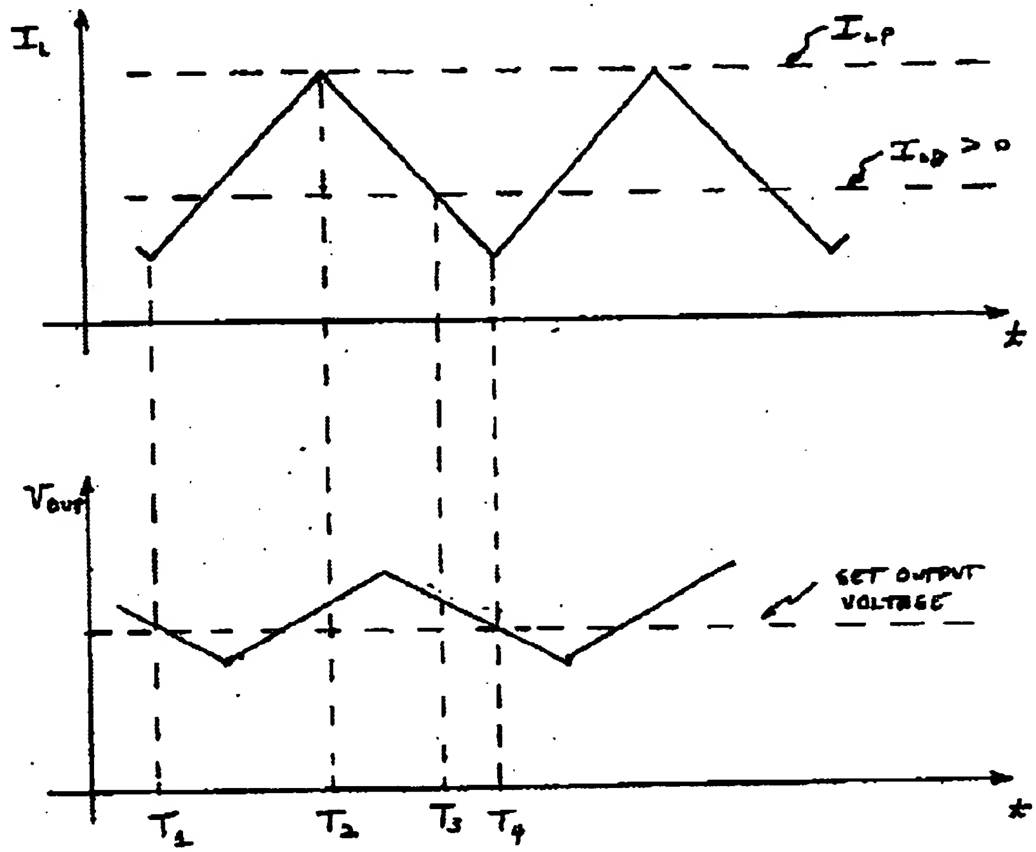
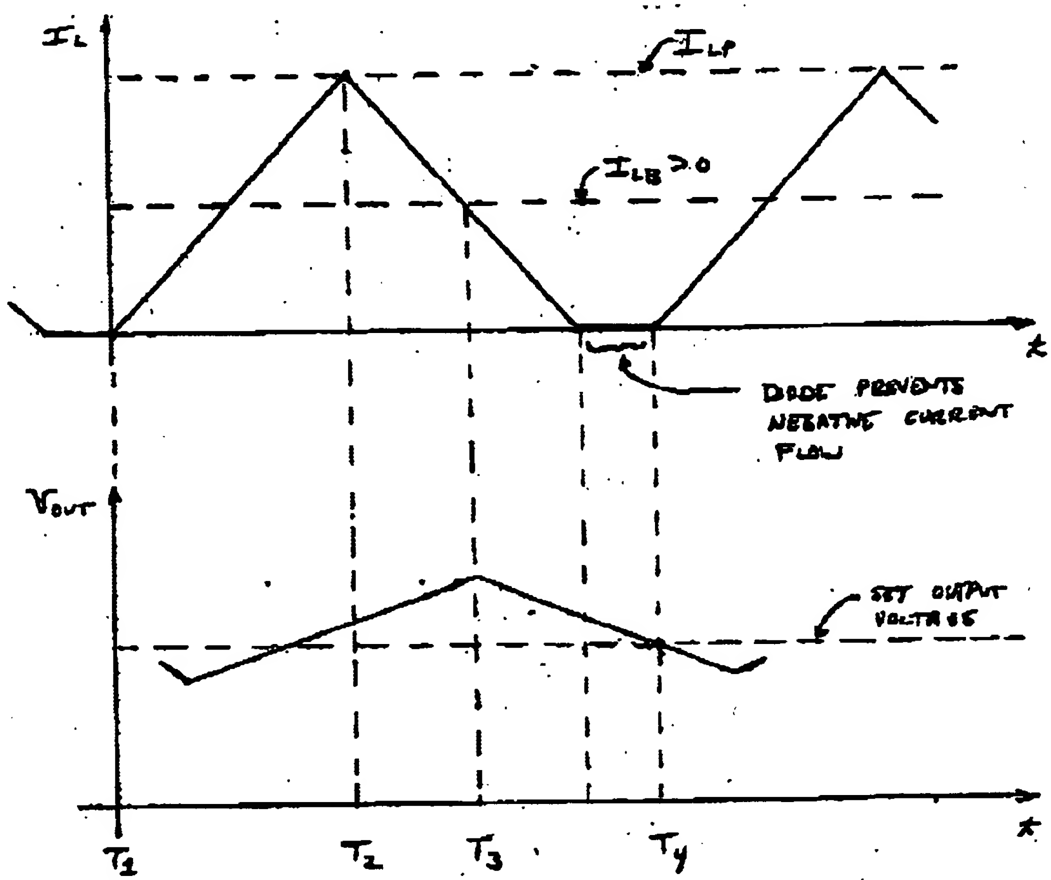
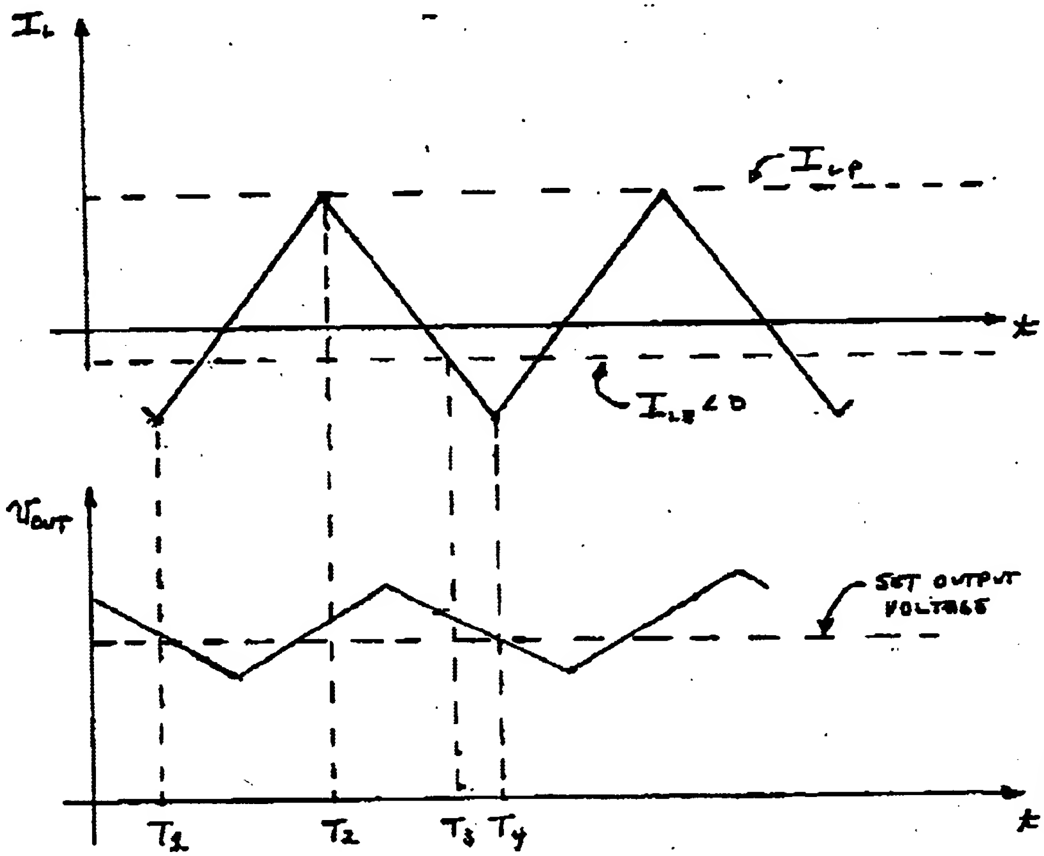


SKETCH 1: $I_{LB} > 0$. HIGHER LOAD CURRENT



SKETCH 2: $I_{LB} > 0$. LOWER LOAD CURRENT
DIODE PREVENTS NEGATIVE CURRENT FLOW



SKETCH 3: $I_{LB} < 0$. SYNCHRONOUS RECTIFIER REPLACES DIODE.